Design Review 1

**Progress**

Our group has made substantial progress towards completing the project. We have successfully set up all of the libraries and models for both the CMOS and FinFET technologies, decided on what designs to use to compare these technologies (NOR, NAND, XOR, Flip Flop, Adder, and MUX), decided on what metrics to use for the comparisons, created all of our designs, and have measured the propagation delay for all of these designs. We have mostly kept to our timeline, but are a little bit behind on the power consumption measurements. However, this will not hinder us on completing the project on time.

**Challenges**

The biggest challenge that we ran into was setting up the library for the FinFET technology. We kept getting errors in Cadence indicating that the libraries were unable to be loaded. Eventually we discovered that the path of the libraries had been changed and no longer matched the path that the tutorial had on the wiki. Once we discovered this, we changed the path and the problem was solved. This was the only challenge we faced.

**Remaining Tasks**

In order to complete the project, we need to measure the power consumption for our NOR, XOR, Flip Flop, and MUX designs for both the CMOS and FinFET technologies. We also need to find a good way to accurately measure the area for our designs.